# Efficient Building Blocks for Reversible Sequential Circuit Design

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*Abstract*— Reversible logic is gaining interest in the recent past due to its less heat dissipating characteristics. It has been proved that any Boolean function can be implemented using reversible gates. In this paper we propose a set of basic sequential elements that could be used for building large reversible sequential circuits leading to logic and garbage reduction by a factor of 2 to 6 when compared to existing reversible designs reported in the literature.

*Keywords:* Reversible Logic, Reversible Gate, Power Dissipation, Flip-Flop, Garbage.

## I. INTRODUCTION

Energy dissipation is becoming a major barrier in the evolving nano-computing era. As reversible logic ensures low energy dissipation [1][2] it has gained importance in the recent past. An operation is said to be physically reversible if there is no energy to heat conversion and no change in entropy. On same lines, reversible logic computation implies that no information about the computational state can ever be lost. R. Landauer [3] has shown that for every bit of information that is erased during an irreversible logic computation $kTln2$ joules of heat energy is generated, where k is the Boltzmann constant and $T$ is the temperature in kelvin at which the system is operating. C. H. Bennett [4] showed that the $kTln2$ amount of energy dissipation would not occur if a computation is carried out in a reversible way.

A reversible gate is a logical cell that has the same number of inputs and outputs with a bijective mapping between the input and output vectors. Direct fan-outs from the reversible gate and feedbacks from a gate output directly to its inputs are not permitted. A reversible gate with $n$-inputs and $n$-outputs is called a $n \times n$ reversible gate. An elaborate list of reversible gates studied in the literature is presented in [5]. Some prominent among them are the Feynman gate [6] (Figure 1(a)), the Toffoli Gate [7] (Figure 1(b)), the Fredkin gate [8] (Figure 1(c)), the Kerntopf gate [5] and the Margolus gate [9].

Some of the prominent CMOS-based implementation techniques for reversible circuits reported in the literature include the Charge Recovery Logic (CRL) [10], the Split-Level Charge Recovery Logic (SCRL) [11], the Reversible Energy Recovery
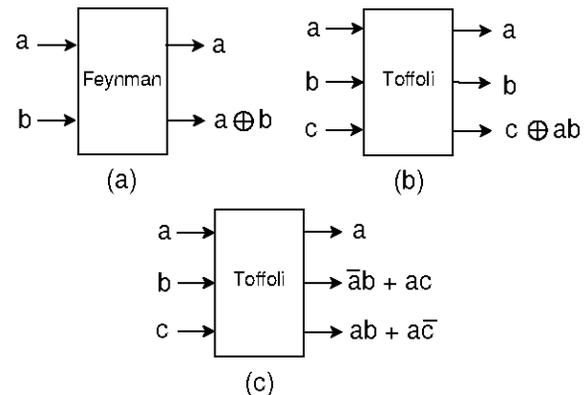


Fig. 1.    Reversible Gates: (a) Feynman (b) Toffoli (c) Fredkin

Logic (RERL) circuits [12] [13] and the nMOS Reversible Energy Recovery Logic (nRERL) [14]. In addition, opto-electronic and nanoelectronic implementations of reversible gates were also found in the literature [15] [16]. There is relatively little progress in the synthesis of reversible gates. A comprehensive survey of synthesis techniques for reversible logic along with a binary decision diagram-based incremental algorithm for reversible logic synthesis is presented in [17]. An important metric for evaluating reversible circuits is the *Garbage* count. Garbage is defined as the number of outputs added to make an $n$-input $k$-output Boolean function $((n, k)$ function) reversible [18]. Hence, one of the major issues in designing a reversible circuit is *garbage minimization*.

## II. AN UNIVERSAL REVERSIBLE GATE

In this section we propose a new universal reversible logic gate as shown in Figure 2. The truth table for the same as shown in Table I, implies a bijective mapping between the input and output vectors. Hence, the gate is reversible. It is easy to infer from Figure 2 that by setting input $c$ to logic 0, the $AND$ and $OR$ functions of $a$ and $b$ are realized at outputs $o_1$ and $o_3$ respectively. Similarly, by setting input $c$ to logic 1, the $NAND$ and $NOR$ functionalities can be realized.

There are certain important advantages of this new gate.

It has been proved that realizing both $NOR$ and $NAND$ functionalities on the same reversible gate is advantageous for synthesizing multivalued reversible logic [5]. Apart from this, the gate proves to be very handy for designing sequential elements like the RS latch as discussed in the following sections. In the rest of this paper $URG$ will denote the proposed reversible gate shown in Figure 2.
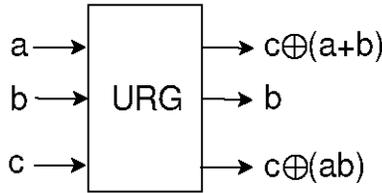


Fig. 2.   The New Gate (G)

| a | b | c | $o_1$ | $o_2$ | $o_3$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 |

TABLE I

TRUTH TABLE NEW GATE (G)

## III. REVERSIBLE SEQUENTIAL CIRCUITS

Very little previous research has been done on designing sequential circuits using reversible logic. Synthesis of sequential circuits is very different from that of combinational circuits. The difficulty arise from the fact that sequential circuits require a feedback from one of the outputs and reversible logic gates do not allow a fan-out of more than one. The most recently reported work [19] in this topic focuses on the construction of reversible sequential circuits by replacing the irreversible gates of a normal irreversible sequential circuit with the appropriate reversible gates. The study did not focus on the optimization in terms of logic gates and garbage minimization. In this paper we propose a set of basic sequential elements that could be used for building large reversible sequential circuits leading to logic and garbage reduction by a factor of 2 to 6 when compared to those proposed in [19].

## IV. RS LATCH

In this section we propose reversible circuit designs for RS Latch. The $NOR$ Latch circuit is shown in Figure 3(a). Each $NOR$ gate is replaced with $URG$ and the circuit design is shown in Figure 3(b). The circuit shown in Figure 3(c) is a basic $NAND$ Latch. The reversible $NAND$ Latch design using the Toffoli gate is shown in Figure 3(e) and the design using $URG$ is shown in Figure 3(d).

| | No. of Gates | Garbage outputs |
|---|---|---|
| Proposed Design | 2 | 2 |
| Existing Design | 4 | 4 |
| Improvement factor | 2 | 2 |

TABLE II

COMPARISON OF PROPOSED RS LATCH WITH EXISTING DESIGN

The advantage of using $URG$ is that we can design both the $NAND$ Latch and $NOR$ Latch using the same basic unit. The existing design did not utilize the same output coming out of the reversible gate. Instead they were explicitly producing an additional fan-out by using an extra reversible gate making the circuit complex and costly. The comparison of the proposed design and the existing design is shown in Table II
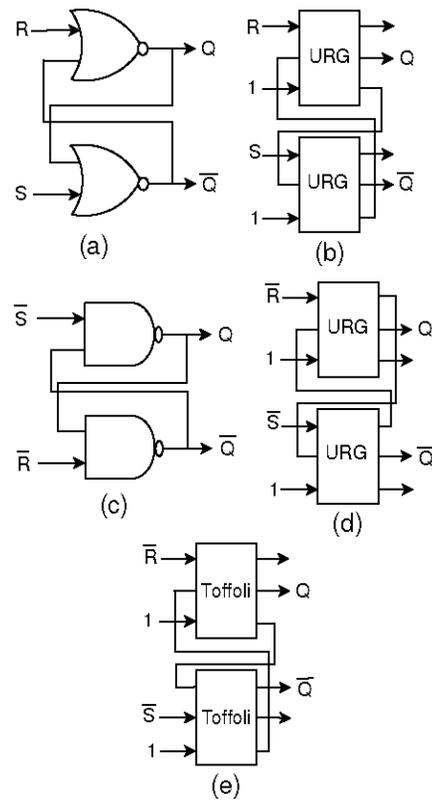


Fig. 3.   Latches (a) NOR (b) Reversible NOR (c) NAND (d) Reversible NAND (e) Reversible NAND latch using toffoli

## V. D FLIP-FLOP

In this section we design a reversible positive level triggered D Flip-Flop. The truth table of a D Flip-Flop is shown in Table III. The design of the D Flip-Flop is shown in Figure 4. A Fredkin gate is used as a 2:1 mux and the Feynman gate is used for getting fan-out of 2.

Similarly, we design a negative level triggered D Flip-Flop. The design of the negative level triggered D Flip-Flop is shown in Figure 5. The power of the Fredkin gate that it can act as a 2:1 mux for both the select and the $NOT$ of select at the

| enable | d | Q |
|--------|---|------|
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| 0 | x | Q(t-1) |

TABLE III

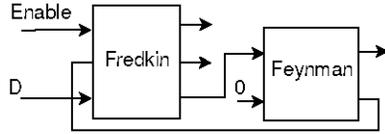POSITIVE LEVEL TRIGGERED DATA FLIP-FLOP



Fig. 4.   Reversible positive level triggered D Flip-Flop

same time has been exploited.

The proposed design requires less number of logic gates and the garbage generated is also lesser as compared to the older designs. Table IV compares the proposed design and the existing design. If we design the D Flip-Flop by using the design of the RS and by setting R and S values appropriately we incur a large complexity in the circuit, hence we have designed the circuit from the logic and did not extend the design of RS Latch.

## VI. JK FLIP-FLOP

In this section we design a reversible level triggered JK Flip-Flop. The truth table for a JK Flip-Flop is shown in Table V. From the truth table we see that the JK Flip-Flop is same as D Flip-Flop with $D = J\bar{Q} + \bar{K}Q$.

By observing the formula $J\bar{Q} + \bar{K}Q$ we see that it is a 2:1 mux with inputs as $J$ and $\bar{K}$ and select line as $Q$. Hence, we place a Fredkin gate and a Feynman gate for getting $NOT$ of $K$. The design of positive level triggered JK Flip-Flop is shown in Figure 6. Similarly, we can design a negative level triggered $JK$ Flip-Flop.

The proposed designs require less number of logic gates compared to older designs and the garbage generated by the proposed design is also much less than the existing design. Table VI compares the proposed design and the existing design. If we design the JK Flip-Flop by using the design of
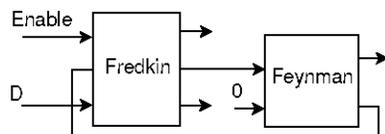


Fig. 5.   Reversible negative level triggered D Flip-Flop

|  | No. of Gates | Garbage outputs |
|--------------------|--------------|-----------------|
| Proposed Design | 2 | 2 |
| Existing Design | 7 | 8 |
| Improvement factor | 3.5 | 4 |

TABLE IV

COMPARISON OF PROPOSED D FLIP-FLOP WITH EXISTING DESIGN

| enable | j | k | Q |
|--------|---|---|-----------|
| 1 | 0 | 0 | no-change |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | Toggle |
| 0 | x | x | no-change |

TABLE V

POSITIVE LEVEL TRIGGERED JK FLIP-FLOP

|  | No. of Gates | Garbage outputs |
|--------------------|--------------|-----------------|
| Proposed Design | 4 | 4 |
| Existing Design | 10 | 12 |
| Improvement factor | 2.5 | 3 |

TABLE VI

COMPARISON OF PROPOSED JK FLIP-FLOP WITH EXISTING DESIGN

the RS and by setting R and S values appropriately we incur a large complexity in the circuit. Hence we have designed the circuit from the logic and did not extend the design of RS Latch.
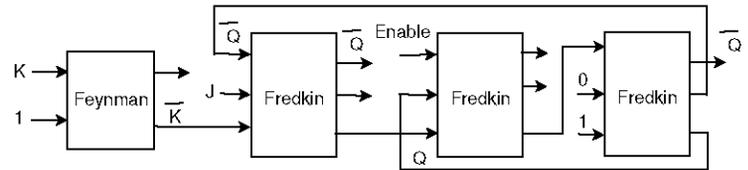


Fig. 6.   Reversible positive level triggered JK Flip-Flop

## VII. T FLIP-FLOP

In this section we design a reversible level triggered T Flip-Flop. From the truth table of T Flip-Flop (Table VII) we can say that the T Flip-Flop is same as D Flip-Flop with $D = T \oplus Q$.

Hence, by utilizing the efficient design of D Flip-Flop we construct a T Flip-Flop by adding the functionality to D. The $XOR$ functionality is added by a single Feynman gate. The design of positive level triggered T Flip-Flop is shown in Figure 7. Similarly, we can design a negative level triggered T Flip-Flop. The proposed design requires lesser number of logic gates and the garbage generated is also less as compared to the existing design. Table VIII compares the proposed design and the existing design.

| enable | t | $Q(t-1)$ | Q |
|--------|---|----------|-----------|
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 0 | x | x | no-change |

TABLE VII

POSITIVE LEVEL TRIGGERED T FLIP-FLOP
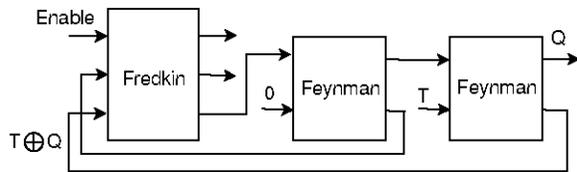
Fig. 7.   Reversible positive level triggered T Flip-Flop

| | No. of Gates | Garbage outputs |
|---|---|---|
| Proposed Design | 3 | 2 |
| Existing Design | 10 | 12 |
| Improvement factor | 3.3 | 6 |

TABLE VIII

COMPARISON OF PROPOSED T FLIP-FLOP WITH EXISTING DESIGN

## VIII.  MASTER-SLAVE D FLIP-FLOP

In this section we propose the construction of Master-Slave edge triggered D Flip-Flop using reversible gates. The construction of a the master-slave D Flip-Flop is shown in Figure 8. The truth table of the positive edge triggered D Flip-Flop is shown in Table IX. It can be easily verified that the constructions meets the desired characteristics of the positive edge triggered D Flip-Flop. Similarly, we can construct the negative edge triggered D Flip-Flop.

There is no explicit mention of the reversible edge triggered D Flip-Flop. If we do the naive construction by replacing every irreversible gate by appropriate reversible gate, then the number of gates in the design will be 16 and the garbage outputs will be 17. The comparison is shown in the Table X.

## IX.  MASTER-SLAVE JK FLIP-FLOP

In this section we propose the construction of Master-Slave JK Flip-Flop using reversible gates. The truth table is shown in Table XI. The design is shown in the Figure 9. We added a Fredkin gate and a Feynman gate to get the functionality of $J\bar{Q} + \bar{K}Q$. The comparison of the proposed design with the existing ones is shown in the Table XII.
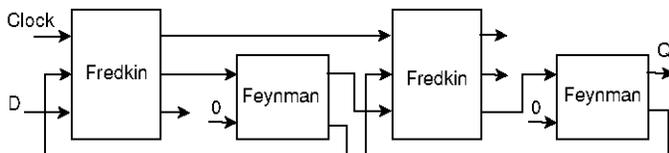


Fig. 8.   Reversible positive edge triggered D Flip-Flop

| Clock | d | $Q(t)$ |
|---|---|---|
| pos-edge | 0 | 0 |
| pos-edge | 1 | 1 |
| neg-edge | x | Q(t-1) |

TABLE IX

POSITIVE EDGE TRIGGERED DATA FLIP-FLOP

| | No. of Gates | Garbage outputs |
|---|---|---|
| Proposed Design | 4 | 3 |
| Existing Design | 16 | 17 |
| Improvement factor | 4 | 5.66 |

TABLE X

COMPARISON OF PROPOSED MASTER-SLAVE D FLIP-FLOP WITH EXISTING DESIGN

| Clock | j | k | $Q$ |
|---|---|---|---|
| pos-edge | 0 | 0 | no-change |
| pos-edge | 0 | 1 | 0 |
| pos-edge | 1 | 0 | 1 |
| pos-edge | 1 | 1 | Toggle |
| neg-edge | x | x | no-change |

TABLE XI

POSITIVE EDGE TRIGGERED JK FLIP-FLOP

## X.  MASTER-SLAVE T FLIP-FLOP

In this section we propose the construction of Master-Slave T Flip-Flop using reversible gates. The truth table is shown in the Table XIII. The design is shown in the Figure 10. We added a Feynman gate to get the desired functionality of $T \oplus Q$. The comparison of the proposed design with the existing ones is shown in the Table XIV.

There is no explicit mention of the reversible edge triggered T Flip-Flop. If we do the naive construction by replacing every irreversible gate by appropriate reversible gate, then the number of gates in the design and the garbage outputs will be 18. The comparison is shown in the Table XIV.

## XI.  CONCLUSIONS

The paper proposed the design of a new reversible logic gate which is shown to be advantageous for synthesizing multivalued reversible logic [5]. The proposed reversible gate is utilized for efficiently designing the RS latch. The paper proposes the designs of the reversible Flip-Flops and Latch using the proposed gate, Fredkin gate, Toffoli gate

| | No. of Gates | Garbage outputs |
|---|---|---|
| Proposed Design | 6 | 6 |
| Existing Design | 18 | 21 |
| Improvement factor | 3 | 3.5 |

TABLE XII

COMPARISON OF PROPOSED MASTER-SLAVE JK FLIP-FLOP WITH EXISTING DESIGN

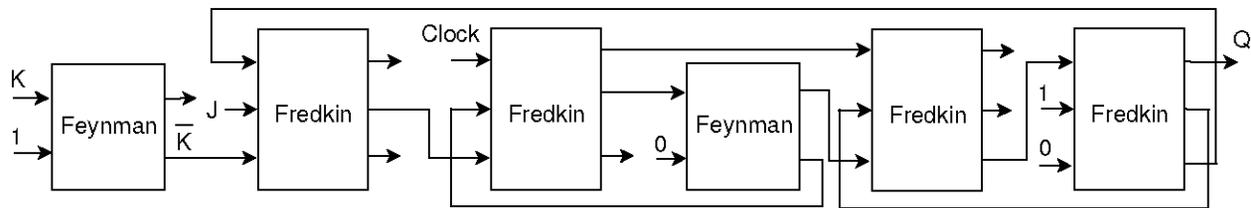| Clock | T | $Q(t)$ |
|---|---|---|
| pos-edge | 0 | Q(t-1) |
| pos-edge | 1 | Q(t-1) |
| neg-edge | x | Q(t-1) |

TABLE XIII

POSITIVE EDGE TRIGGERED T FLIP-FLOP

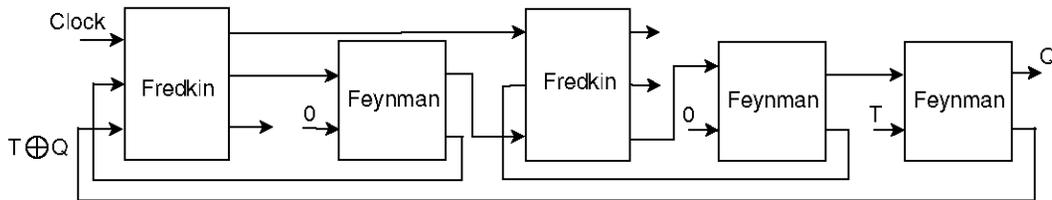Fig. 9. Reversible positive edge triggered JK Flip-Flop



Fig. 10. Reversible positive edge triggered T Flip-Flop

|  | No. of Gates | Garbage outputs |
|---|---|---|
| Proposed Design | 5 | 3 |
| Existing Design | 18 | 18 |
| Improvement factor | 3.6 | 6 |

TABLE XIV

COMPARISON OF PROPOSED MASTER-SLAVE T FLIP-FLOP WITH

EXISTING DESIGN

and the Feynman gate. The designs are compared with the existing design and are shown to be have an improvement by a factor of 2 to 6. The proposed designs utilized the fact that the reversible circuits constructed from the logic are better in terms of logic complexity and garbage minimization than the one obtained by converting the irreversible designs by replacing gates appropriately. The proposed designs are highly optimized. The number of garbage outputs generated and the number of gates used in the designs are very small as compared to the earlier implementations.

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